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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/756,177	GAMBINO ET AL.	
	Examiner	Art Unit	
	Hung K. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-11 and 50-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-11 and 50-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 5-11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 respectively, of U.S. Patent No. 6,252,271. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 5-11, 51 and 62 are generic to claims 1-7 of U.S. Patent No. 6,252,271. The claimed invention (claims 5-11) of the present application is a mere broader version of the

claimed invention (claims 1-6) of the above identified U.S. Patent with similar intended scope, thus allowing unjustified or improper timewise extension of the "right to exclude" granted by a U.S. Patent No. 6,252,271. Note that claim 5 has the similar intended scope (substantially vertical sidewall) as claims 1 and 6 of Patent No. '271, claim 51 has the similar intended scope ("same level" has the same meaning as "co-planar") as claim 7 of Patent No. '271, and claim 62 has the similar intended scope as claim 1 of Patent No. '271

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 5, 8 – 11, 50, 52, 55 – 57 and 59 – 61 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. (PN 5,633,519, of record).

Yamazaki et al. discloses, as shown in Figures 1(A)-1(B) and 3(E), a memory comprising,

a gate conductor (104) comprising a first side and a second side, the first side comprising a slope and the second side comprising a substantially vertical sidewall;

at least one floating gate (103) comprising polysilicon spacer material [Col. 9, lines 1-3] and formed on the second side of the gate conductor such that the gate conductor surrounds the at least one floating gate on a plurality of sides.

With regard to claims 8 and 11, Yamazaki et al. discloses the gate conductor surrounds the at least one floating gate on at least two sides [see Figures 1(B)].

With regard to claim 9, Yamazaki et al. discloses the gate conductor surrounds the at least one floating gate on three sides [see Figures 1(B)].

With regard to claim 10, Yamazaki et al. discloses the at least one floating gate is self-isolated from an adjacent floating gate by the gate conductor [see Figures 1(B)].

With regard to claim 50, Yamazaki et al. discloses the floating gate formed on the gate conductor comprises a single sidewall structure. Note that the claimed language does not specifically state that only a single sidewall structure formed on the gate conductor [Figures 1(A)-1(B) and 3(E)].

With regard to claim 52, Yamazaki et al. discloses the gate conductor comprises a control gate [Figures 1(A)-1(B) and 3(E)].

With regard to claim 55, Yamazaki et al. discloses the first side comprises a tapered sidewall [Figures 1(A)-1(B) and 3(E)].

With regard to claim 56, Yamazaki et al. discloses the memory further comprising an oxide layer formed on the second side and having a substantially uniform thickness [Figures 1(A)-1(B) and 3(E)].

With regard to claim 57, Yamazaki et al. discloses the memory further comprising a tunneling region formed underneath the floating gate [Figures 1(A)-1(B) and 3(E)].

With regard to claim 59, Yamazaki et al. discloses the second side comprises a notch side having three sidewalls, the floating gate being formed on the three sidewalls [Figures 1(A)-1(B) and 3(E)].

With regard to claim 60, Yamazaki et al. discloses the gate conductor comprises an active area (101), and wherein the floating gate overlaps the active area by a predetermined minimum dimension to provide a predetermined threshold voltage [Figures 1(A)-1(B) and 3(E)].

With regard to claim 61, Yamazaki et al. discloses an oxide sidewall is formed on the gate conductor [Figures 1(A)-1(B) and 3(E)].

3. Claims 5, 8 – 11, 50, 52, 55 – 57 and 59 – 61 are rejected under 35 U.S.C. 102(b) as being anticipated by Yang (PN 5,258,634, of record).

Yang discloses, as shown in Figures 5C-8, a memory comprising,

a gate conductor (24) comprising a first side and a second side, the first side comprising a slope and the second side comprising a substantially vertical sidewall;

at least one floating gate (17) comprising polysilicon spacer material [Col. 2, lines 52-54] and formed on the second side of the gate conductor such that the gate conductor surrounds the at least one floating gate on a plurality of sides.

With regard to claims 8 and 11, Yang discloses the gate conductor surrounds the at least one floating gate on at least two sides [see Figures 5C-8].

With regard to claim 9, Yang discloses the gate conductor surrounds the at least one floating gate on three sides [see Figures 5C-8].

With regard to claim 10, Yang discloses the at least one floating gate is self-isolated from an adjacent floating gate by the gate conductor [see Figures 5C-8].

With regard to claim 50, Yang discloses the floating gate formed on the gate conductor comprises a single sidewall structure. Note that the claimed language does not specifically state that only a single sidewall structure formed on the gate conductor [Figures 5C-8].

With regard to claim 52, Yang discloses the gate conductor comprises a control gate [Figures 5C-8].

With regard to claim 55, Yang discloses the first side comprises a tapered sidewall [Figures 5C-8].

With regard to claim 56, Yang discloses the memory further comprising an oxide layer formed on the second side and having a substantially uniform thickness [Figures 5C-8].

With regard to claim 57, Yang discloses the memory further comprising a tunneling region formed underneath the floating gate [Figures 5C-8].

With regard to claim 59, Yang discloses the second side comprises a notch side having three sidewalls, the floating gate being formed on the three sidewalls [Figures 5C-8].

With regard to claim 60, Yang discloses the gate conductor comprises an active area (101), and wherein the floating gate overlaps the active area by a predetermined minimum dimension to provide a predetermined threshold voltage [Figures 5C-8].

With regard to claim 61, Yang discloses an oxide sidewall is formed on the gate conductor [Figures 5C-8].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 53 – 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (PN 5,633,519, of record) in view of Wake (PN 5,338,953, of record). Yamazaki et al. discloses the invention as claimed, including the memory as cited in the rejections of claim 5. Yamazaki et al. further discloses the gate conductor is formed on a silicon substrate (no label, or 301,401), and adjacent ones of the at least one floating gate are isolated from each other and the second side includes regions provided between the adjacent ones of the at least one floating gate. Yamazaki et al. does not disclose regions are tapered. However, Wake discloses a second side of a gate conductor (7) having tapered regions provided between the adjacent ones of the at least one floating gate (5). Note Figures 3 and 18 of Wake. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the second side of Yamazaki et al. having tapered regions, such as taught by in order to reduce the mask processes.

With regard to claim 53, Yamazaki et al. and Wake disclose an angle between the first side and the substrate is less than 90 degrees [Figures 1(A)-1(B) and 3(E)].

With regard to claim 54, Yamazaki et al. and Wake disclose the angle is between about 45 degrees to 60 degrees.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang (PN 5,258,634, of record) in view of Wake (PN 5,338,953, of record).

Yang discloses the invention as claimed, including the memory as cited in the rejections of claim 5. Yang further discloses the gate conductor is formed on a silicon substrate (10), and adjacent ones of the at least one floating gate are isolated from each other and the second side includes regions provided between the adjacent ones of the at least one floating gate. Yang does not disclose regions are tapered. However, Wake discloses a second sidewall of a gate conductor (7) having tapered regions provided between the adjacent ones of the at least one floating gate (5). Note Figures 3 and 18 of Wake. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the second side of Yang having tapered regions, such as taught by in order to reduce the mask processes.

6. Claims 7 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (PN 5,633,519, of record).

With regard to claim 7, Yamazaki et al. discloses the invention as claimed, including the memory as cited in the rejections of claim 5. Yamazaki et al. further discloses the gate conductor surrounds the at least one floating gate on the plurality of sides. Yamazaki et al. does not disclose the gate conductor surrounds the at least one floating gate on only two sides. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form gate conductor of Yamazaki et al. surrounding on only two sides in order to simplify the process steps and to have a desired pattern.

With regard to claim 58, Yamazaki et al. discloses the invention as claimed, including the memory as cited in the rejections of claim 5. Yamazaki et al. further discloses the gate

conductor is covered by a dielectric. Yamazaki et al. does not disclose the dielectric comprising a thickness in a range of about 100 nm to 1,000 nm. Although Yamazaki et al. does not teach the thickness of the dielectric, as that claimed by Applicants, however, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the dielectric having a desired thickness, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

7. Claims 7 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang (PN 5,258,634, of record).

Yang discloses the invention as claimed, including the memory as cited in the rejections of claim 5. Yang further discloses the gate conductor surrounds the at least one floating gate on the plurality of sides. Yang does not disclose the gate conductor surrounds the at least one floating gate on only two sides. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form gate conductor of Yang surrounding on only two sides in order to simplify the process steps and to have a desired pattern.

With regard to claim 58, Yang discloses the invention as claimed, including the memory as cited in the rejections of claim 5. Yang further discloses the gate conductor is covered by a dielectric. Yang does not disclose the dielectric comprising a thickness in a range of about 100 nm to 1,000 nm. Although Yang et al. does not teach the thickness of the dielectric, as that claimed by Applicants, however, it would have been obvious to one having ordinary skill in the art at the

time the invention was made to form the dielectric having a desired thickness, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

8. Applicant's arguments filed 09/22/03 have been fully considered but they are not persuasive.

It is argued, at pages 9 – 10 of the Remarks, that nowhere does the '271 Patent indicate a substantially vertical sidewall or the gate conductor surrounds at least one floating gate. This argument is not convincing because claims 1 and 6 of the '271 Patent indicates a substantially vertical sidewall and at least one floating gate is partially surrounded on a plurality of sides by the second sidewall of the word line (which also is the gate conductor).

It is argued, at pages 9 – 10 of the Remarks, that this present invention is a Divisional Application of U.S. Patent Application 09/097,515 (Parent Application), now Patent No. 6,252,271 and that Applicant elected to file the Divisional Application for claims 5-11 as the Examiner previously indicated that claims 5-11 of the Parent Application represented a different invention than the invention defined by claims 1-4 of the same Parent Application, so that claims 1-4 and 5-11 of the Parent Application were considered to be two different inventions, the two sets of claims cannot now represent the same invention. This argument is not convincing because in the Parent Application, the Examiner made the restriction based on the two groups of method used to form the device. It was Applicant to elect to exam claims 1-4.

It is argued, at pages 10 – 11 of the Remarks, that Yamazaki et al. discloses the non-volatile floating gate being a symmetric structure with a floating gate and a control gate formed with the gate extending beyond the lower edge of the floating gate electrode, compared to "just a floating gate formed on a side of a gate conductor where the other side of the gate conductor includes a sloped surface". This argument is not convincing because Yamazaki et al. discloses, as shown in Figures 1 and 3(E), a floating gate (103) formed on a side of a gate conductor (104) where the other side of the gate conductor includes a sloped surface. Note that the word "just" does not necessary mean "only".

It is argued, at pages 10 – 12 of the Remarks, that Yamazaki et al. does not disclose at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides since the floating gate, itself, of the present invention is formed on the gate conductor where the gate conductor (control gate) surrounds the floating gate as a result of the notching process whereas Yamazaki et al. teaches a floating gate and a control gate formed on the sidewall to produce a double sidewall. This argument is not convincing because Yamazaki et al. discloses, as shown in Figures 1(A), 1(B) and 3(E), at least one floating gate (103) which includes polysilicon spacer material formed on the second side of the gate conductor (104) such that the gate conductor surrounds at least one floating gate on a plurality of sides. Note that the features upon which applicant relies (i.e., "the floating gate is formed without use of a sloped sidewall", "the floating gate is not self-aligned", and "as a result of the notching process") are

not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is argued, at pages 13 – 14 of the Remarks, that Yang discloses the non-volatile floating gate being a symmetric structure with a floating gate and a control gate formed with the gate extending beyond the lower edge of the floating gate electrode, compared to "just a floating gate formed on a side of a gate conductor where the other side of the gate conductor includes a sloped surface". This argument is not convincing because Yang discloses, as shown in Figures 5C-8, a floating gate (17) formed on a side of a gate conductor (24) where the other side of the gate conductor includes a sloped surface. Note that the word "just" does not necessary mean "only".

It is argued, at pages 10 – 12 of the Remarks, that Yang does not disclose at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides since the floating gate, itself, of the present invention is formed on the gate conductor where the gate conductor (control gate) surrounds the floating gate as a result of the notching process whereas Yang teaches a floating gate and a control gate formed on the sidewall to produce a double sidewall. This argument is not convincing because Yang discloses, as shown in Figures 5C-8, at least one floating gate (17) which includes polysilicon spacer material formed on the second side of the gate conductor (24) such that the gate conductor surrounds at least one

floating gate on a plurality of sides. Note that the features upon which applicant relies (i.e., "the floating gate is formed without use of a sloped sidewall", "the floating gate is not self-aligned", and "as a result of the notching process") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Note that Yamazaki et al., Yang and Wake all teach non-volatile memory device.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

It is argued, at pages 18 – 19 of the Remarks, that Yamazaki et al. does not the gate conductor surrounds at least one floating gate on only two sides. This argument is not

convincing because one of ordinary skill in the art at the time the invention was made would be motivated to form gate conductor of Yamazaki et al. surrounding on only two sides in order to simplify the process steps and to have a desired pattern.

It is argued, at pages 19 – 20 of the Remarks, that Yang does not the gate conductor surrounds at least one floating gate on only two sides. This argument is not convincing because one of ordinary skill in the art at the time the invention was made would be motivated to form gate conductor of Yang surrounding on only two sides in order to simplify the process steps and to have a desired pattern.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

December 12, 2003

Hung Vu

Patent Examiner